

<b>Form PTO-1449</b>  <b>INFORMATION DISCLOSURE CITATION IN AN APPLICATION</b>  <i>(Use several sheets if necessary)</i>				Docket Number 204552016501		Application Number NEW	
				Applicant  <div style="text-align: center; font-weight: bold;">Yuichi SATO</div>			
				Filing Date February 10, 2004		Group Art Unit	
				Mailing Date February 10, 2004			
U.S. PATENT DOCUMENTS							
Examiner Initials	Ref. No.	Date	Document No.	Name	Class	Subclass	Filing Date If Appropriate
D Lee	1.	7/1998	5,780,899	Hu et al.			
	2.	11/1998	5,831,899	Wang et al.			
	3.	9/1999	5,960,289	Tsui et al.			
	4.	2/2000	6,020,222	Wollesen			
FOREIGN PATENT DOCUMENTS							
Examiner Initials	Ref. No.	Date	Document No.	Country	Class	Subclass	Translation YES NO
D Lee	5.	3/1979	JP-A-54-037544	Japan			abs.
	6.	8/1986	JP-A-61-185972	Japan			abs.
	7.	1/1991	JP3022476	Japan			abs.
	8.	2/1992	JP-A-04-053090	Japan			abs.
	9.	6/1995	JP-A-07-161844	Japan			abs.
	10.	5/1996	JP-A-07-176633	Japan			abs.
	11.	8/1998	JP-A-10-222985	Japan			abs.
OTHER DOCUMENTS <span style="float: right; font-size: small;">(including author, title, Date, Pertinent Pages, Etc.)</span>							
Examiner Initials	Ref. No.	Title					
D Lee	12.	"PRINCIPLES OF CMOS VLSI DESIGN", A Systems Perspective, Second Edition, , Neil H.E. Weste and Kamran Eshraghian, Chapter 10, pp 578-83, 1992					
	13.	F. Assaderaghi et al., "Dynamic threshold-voltage MOSFET (DTMOS) for ultra-low voltage VLSI", IEEE Transactions on Electron Devices, vol. 44, no. 3, pp. 414-422, March 1997					
	14.	Assaderaghi et al., 1994 "A dynamic threshold voltage MOSFET (DTMOS) for very low voltage operation" IEEE Electron Device Letters Vol. 15, pp 510-512.					
	15.	Andoh et al., 1994 "Design methodology for low-voltage MOSFETS" IEEE International Electron Devices Meeting, Technical Digest, pp 79-82.					
	16.	Assaderaghi et al., 1994 "A dynamic threshold voltage MOSFET (DTMOS) for ultra-low voltage operation" IEEE International Electron Devices Meeting, Technical Digest, pp 809-812.					
	17.	David A. Hodges et al., "Analysis and design of digital integrated circuits", second edition, McGraw-Hill, Inc., PP 368-369; 1988					
EXAMINER: <i>Douglas Little</i>		1 DATE CONSIDERED: <i>4 Feb 05</i>					
EXAMINER: Initial if citation considered, whether or not the citation conforms with MPEP 609. Draw a line through the citation if not in conformance and not considered. Include a copy of this form with next communication to applicant.							